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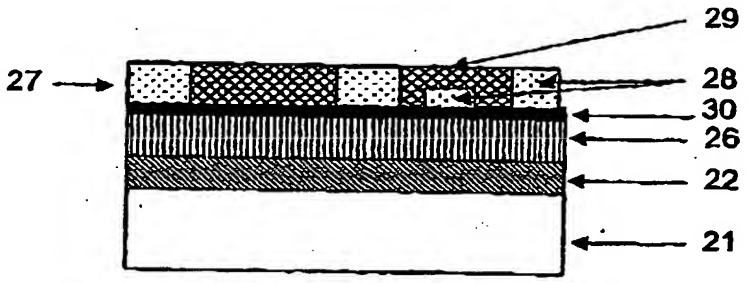
(54) Title: FABRICATION METHOD FOR CRYSTALLINE SEMICONDUCTOR FILMS ON FOREIGN SUBSTRATES



(57) Abstract: The invention provides a method of forming a polycrystalline semiconductor film (26) on a supporting substrate (21, 22) of foreign material. The method involves depositing a metal film (23) onto the substrate, forming a film of metal oxide and/or hydroxide (24) on a surface of the metal, and forming a layer of an amorphous semiconductor material (25) over a surface of the metal oxide and/or hydroxide film. The entire sample is then heated to a temperature at which the semiconductor layer is absorbed into the metal layer and deposited as a polycrystalline layer (26) onto the target surface by metal-induced crystallisation. The metal is left as an overlayer (27) covering the deposited polycrystalline layer, with semiconductor inclusions (28) in the metal layer (29). The polycrystalline semiconductor film (26) and the overlayer (27) are separated by a porous interfacial metal oxide and/or hydroxide film (30). The metal in the overlayer and the interfacial metal oxide and/or hydroxide film are then removed with an etch which undercuts the semiconductor inclusions to form freestanding islands. Finally the freestanding semiconductor "islands" are removed from the surface of the polycrystalline semiconductor layer by a lift-off process. There is also provided a method for the formation of a further polycrystalline layer using a polycrystalline layer as a seed layer. The seed layer may be a polycrystalline semiconductor layer formed by the metal induced crystallisation method. The surface of the seed layer is first cleaned to remove any oxides or other contaminants, before forming an amorphous layer of a semiconductor material over the cleaned surface of the seed layer, and heating the substrate, the seed layer and the amorphous layer to crystallise the semiconductor material by solid phase epitaxy.

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FABRICATION METHOD FOR CRYSTALLINE SEMICONDUCTOR FILMS ON FOREIGN SUBSTRATES

Introduction

The present invention relates generally to the formation of thin semiconductor films for electronic device fabrication, and in particular the invention provides a method for the formation of thin *polycrystalline* semiconductor films on foreign substrates, using a thermal budget in each process step that is compatible with the respective foreign substrate. Throughout this text, the term *polycrystalline material* means material that has an average crystal grain size of above 500 nm and the term *thermal budget* relates to the amount of heat applied during a process step (i.e., the area below the temperature-time curve of the process step).

Background of the Invention

Thin films of polycrystalline silicon (pc-Si) on glass or other foreign substrates are very attractive for a wide range of large-area electronic applications, including thin-film photovoltaic (PV) modules, active matrix liquid crystal displays (AMLCDs), and active matrix organic light emitting diode displays (AMOLEDs). Compared to amorphous Si (a-Si) films, their main benefits are higher carrier mobility in display applications and stable energy conversion efficiency and longer product lifetime in PV applications. Generally, one aims to realize c-Si grains with a grain size as large as possible. The use of glass substrates is attractive since they are cheap and transparent. However the limited thermal stability of commercially available low-cost glass substrates severely limits the allowable thermal budget of each fabrication step (as a rule of thumb, the glass temperature must not exceed 650°C if the process lasts 1 hour or more), resulting in the need for a new technology enabling good material quality at these low temperatures.

As the high melting point of semiconductors is a major obstacle for the formation of polycrystalline semiconductor films at low temperature on foreign substrates, past experimental work dealt primarily with the fabrication of *nanocrystalline* (or, equivalently, microcrystalline) material. Such fine-grained (< 500 nm) material is inevitably of rather low electronic quality. An overview of nanocrystalline silicon materials is given by Schropp and Zeman (Schropp and Zeman, "Amorphous and microcrystalline silicon solar cells", Kluwer Academic Publishers, Dordrecht (1998)). One approach for the fabrication of nanocrystalline materials is

hydrogen-diluted plasma-enhanced chemical vapour deposition (PECVD) at a temperature in the range 200-600°C, whereby the hydrogen is beneficial for both the semiconductor growth process and the passivation of dangling crystallographic bonds within grains and at grain boundaries. A drawback of the hydrogen-diluted PECVD approach with regard to the manufacture of devices that require a rather thick semiconductor film (such as crystalline silicon solar cells) is the low deposition rate for nanocrystalline semiconductor material (much less than 1 nm/s in the case of Si).

Compared to nanocrystalline material, polycrystalline material theoretically has a much better electronic quality, however achieving good-quality polycrystalline material at low temperature on a foreign substrate has proven difficult to achieve. Methods for the low-temperature fabrication of polycrystalline semiconductor films on foreign substrates include solid-phase crystallisation of amorphous semiconductor material (Matsuyama et al., "High-quality polycrystalline silicon thin film prepared by a solid phase crystallization method", Journal of Non-Crystalline Solids 198-200, pp. 940-944 (1996).), solution growth (Shi et al., "Solution growth of polycrystalline silicon on glass at low temperatures", Proceedings First World Conference on Photovoltaic Energy Conversion, Hawaii, pp. 1579-1582 (Dec. 1994) (IEEE, New York, 1995).), laser-induced crystallisation of amorphous semiconductor material (Im and Sposili, "Sequential lateral solidification of thin silicon films on SiO_2", Applied Physics Letters 69, pp. 2864-2866 (1996).), and metal-induced (or, equivalently, metal-mediated) crystallisation of amorphous semiconductor material (Nast et al., "Aluminum-induced crystallization of amorphous silicon on glass substrates above and below the eutectic temperature", Applied Physics Letters 73, pp. 3214-3216 Nov. 1998, Widenborg and Aberle, "Surface morphology of poly-Si films made by aluminium-induced crystallisation on glass substrates", Journal of Crystal Growth 242, pp. 270-282 (July 2002), and Jin et. al. "Nickel induced crystallisation of amorphous silicon thin films", Journal of Applied Physics 84, pp. 194-200 (July 1998) .

All of the methods mentioned above have been limited by one or more of the following factors:-

i. long processing times,
ii. rough surfaces,
iii. highly doped films
iv. small grain sizes.

Despite a high level of research interest, none of them has as yet led to a commercially available photovoltaic device. The organisation that has come closest to a commercial low-cost thin-film polycrystalline silicon (pc-Si) photovoltaic product is

Pacific Solar Pty Ltd of Sydney Australia, producing modules at pilot line scale with an efficiency of about 8 %.

For optimum results on foreign substrates, the preparation of polycrystalline material often involves a preliminary step that creates a thin polycrystalline "seed layer" on the substrate, whereby the electronic quality of this seed layer is not critical. Such seed layers can, in principle, be prepared by each of the methods mentioned above.

The metal-induced crystallisation (MIC) process of amorphous semiconductor material as developed at the University of New South Wales (UNSW) (Nast and Hartmann, "Influence of interface and Al structure on layer exchange during aluminum-induced crystallization of amorphous silicon", Journal of Applied Physics 88, pp. 716-724 (July 2000)) is simple and fast and hence has significant industrial appeal. The metal and semiconductor must be chosen such that they can form a eutectic system, enabling crystallisation at low temperature without the formation of metal silicide. However, with respect to using the resulting polycrystalline semiconductor film for the fabrication of electronic devices or as seed layer, a significant problem of the MIC-prepared polycrystalline semiconductor film is the fact that it is covered by an overlayer consisting of metal and semiconductor inclusions, and that between the polycrystalline semiconductor film and the overlayer there exists an interfacial metal oxide and/or metal hydroxide film with which the semiconductor inclusions are in contact and securely connected (Widenborg and Aberle, "Surface morphology of poly-Si films made by aluminium-induced crystallisation on glass substrates", Journal of Crystal Growth 242, pp. 270-282 (July 2002)).

The polycrystalline semiconductor film is of primary interest for device fabrication (such as thin-film transistors) or seed layer applications, and hence the metal+semiconductor overlayer and the metal oxide and/or hydroxide interfacial film must be removed by a suitable processing sequence without significantly thinning or damaging the underlying polycrystalline semiconductor film. A conceivable way to achieve this consists in using a method that simultaneously and uniformly removes the metal+semiconductor overlayer. This has proven to be a very difficult task because, in general, the etching rates for the different components of a composite material, such as the overlayer, are not identical. A possible candidate for this purpose is plasma ion etching. For the Si-Al system, the use of an argon plasma has been tested, however, this has proven unsuccessful due to non-uniform etching. Another possible candidate is reactive ion etching with a chlorine plasma. This process, however, appears unattractive due to its technical complexities, as discussed by Wolf and Tauber (Wolf

and Tauber, "Silicon processing for the VLSI era", Vol. 1, Lattice Press, CA, USA (1986). Pages 559 to 564).

Given the difficulties with the above methods for uniform removal of the metal+semiconductor overlayer, *selective (or non-simultaneous removal)* approaches have been investigated. Teams at UNSW and elsewhere have investigated a wet-chemical method for removal of the metal (see Nast et al, (above) and Niira et al., "Thin film poly-Si formation for solar cells by flux method and Cat-CVD method", Solar Energy Materials and Solar Cells 69, pp. 107-114 (Sep. 2001).). However, because this method does not remove the semiconductor inclusions, this process creates a very rough polycrystalline semiconductor surface that leads to numerous (and virtually insurmountable) problems during subsequent device processing. The creation of this rough surface will very likely have detrimental effects on the electrical performance of the devices or, in the case of seed layer applications, on the structural properties of a subsequently grown polycrystalline semiconductor film.

Solid phase epitaxy (SPE) of semiconductors on *native* substrates is a known deposition method in the literature (see for example A.V. Zotov and V.V. Korobtsov, Journal of Crystal Growth 98 p. 519 (1989).). An amorphous semiconductor (for example silicon) is deposited in ultra-high vacuum onto a cool substrate, which consists of the same semiconductor, and then annealed at a temperature high enough to achieve epitaxial crystallisation. The key feature in SPE is a crystallographic transferral of information from the crystalline substrate into the growing epitaxial film and therefore this method is usually associated with a *native* high-quality crystalline substrate such as a silicon wafer and not with a foreign substrate such as glass.

If the crystalline semiconductor substrate and the epitaxial film consist of the same semiconductor material, the growth method is known in the literature as homo-epitaxy. For two different types of crystalline semiconductor materials which have a close lattice match, a solid phase epitaxial growth is still possible. Such an epitaxial growth by one type of crystalline semiconductor grown on a different crystalline semiconductor substrate is known in the literature as hetero-epitaxy..

Any discussion of documents, acts, materials, devices, articles or the like which has been included in the present specification is solely for the purpose of providing a context for the present invention. It is not to be taken as an admission that any or all of these matters form part of the prior art base or were common general knowledge in the field relevant to the present invention as it existed before the priority date of each claim of this application.

Throughout this specification the word "comprise", or variations such as "comprises" or "comprising", will be understood to imply the inclusion of a stated element, integer or step, or group of elements, integers or steps, but not the exclusion of any other element, integer or step, or group of elements, integers or steps.

Summary of the Invention

According to a first aspect, the present invention consists in a method of preparing a polycrystalline semiconductor film on a supporting foreign substrate, the method comprising:

i. Depositing a metal film onto a target surface of the substrate on which the polycrystalline semiconductor film is to be formed;

ii. Forming a film of metal oxide and/or metal hydroxide on a surface of the metal;

iii. Forming a layer of an amorphous semiconductor material over a surface of the metal oxide and/or metal hydroxide;

iv. Heating the entire sample at a temperature at which the semiconductor layer is absorbed into the metal layer and deposited onto the target surface by metal-induced crystallisation (MIC) as a polycrystalline layer ("MIC polycrystalline layer"), whereby the metal is left as an overlayer covering the deposited polycrystalline layer, with semiconductor inclusions in the metal layer, and the polycrystalline semiconductor film and the overlayer separated by a porous interfacial metal oxide and/or metal hydroxide film with which the semiconductor inclusions are in contact;

v. Removal of the metal in the overlayer and the interfacial metal oxide and/or metal hydroxide film with an etch which under-etches the semiconductor inclusions to form freestanding semiconductor islands weakly connected to the polycrystalline layer, without significantly thinning the underlying polycrystalline semiconductor layer.

vi. Removal of the free-standing semiconductor islands from the surface of the polycrystalline semiconductor layer by a lift-off process.

As the polycrystalline semiconductor will always be highly doped due to metal incorporation, with a doping polarity corresponding to the metal used, a change of the doping polarity of the polycrystalline semiconductor can be induced by suitable process steps. Examples include heating of the polycrystalline semiconductor in the vicinity of a doping source or adding suitable doping impurities in the amorphous semiconductor.

Preferably the substrate provides a planar base on which the semiconductor material is supported. Preferably also a surface on which the semiconductor material is supported is textured to assist light trapping in the semiconductor material.

In some embodiments of the invention the substrate comprises a sheet of a substrate material on which a preliminary layer, such as a thin antireflection layer, is formed, and the target surface is a surface of the preliminary layer, however the target surface may also be a surface of the substrate material on which the process of the present invention is performed directly.

In various embodiments of the invention the substrate is a material selected from the group comprising sapphire, quartz, glass (float, borosilicate and other types), metal, graphite, ceramics, plastics and polymers.

Embodiments of the invention may make use of a semiconductor material selected from the group comprising silicon, germanium, and an alloy of silicon and germanium.

The metal used in various embodiments is selected such that the metal forms a eutectic solution with the selected semiconductor. For example the metal may be selected from the group of metals comprising Be, Al, Zn, Ga, Ag, Cd, In, Sn, Sb and Au. In the preferred embodiment, the semiconductor material is silicon, the metal is aluminium, and the substrate material is glass.

The formation of the metal oxide and/or metal hydroxide film can result in a film of relatively pure metal oxide, a film of relatively pure metal hydroxide, or a mixture of the two. To form an oxide film the metal layer is oxidised in a dry oxygen containing atmosphere (i.e. 0% relative humidity) at room temperature (i.e. 22° ± 1°) for an appropriate period which may vary according to the metal and the concentration of oxygen in the atmosphere. To form a hydroxide film the metal layer is hydro-oxidised in an oxygen containing atmosphere containing 100% relative humidity at room temperature (i.e. 22° ± 1°) for an appropriate period which again may vary according to the metal and the concentration of oxygen in the atmosphere. It is also possible to form a hydroxide film by immersing the aluminium surface into water at room temperature (i.e. 22° ± 1°) or at an elevated temperature. To achieve a mixture of metal oxide and metal hydroxide the process is performed in a semi-dry oxygen containing atmosphere (0% < relative humidity < 100%). For less reactive metals this step may be performed at higher temperatures to speed up the process. The metal oxide and/or metal hydroxide film is preferably formed to a thickness in the range of 2 to 30 nm, however thicker films will also allow the process to work albeit possibly at the cost of longer processing times. The result of a longer exposure time is potentially a thicker

interfacial film which may slow subsequent processing, however as the interfacial film growth is substantially self limiting this is not likely to be a problem. The result of a shorter exposure time will be a thinner and less uniform interfacial film, resulting in a faster and less controllable MIC process and potentially a failure of the etch to fully underetch the islands.

In the preferred embodiment a thin aluminium hydroxide film is grown by hydro-oxidising the surface of the aluminium layer in an air atmosphere containing 100% relative humidity. To form an aluminium hydroxide film of sufficient thickness, the aluminium surface is exposed to air for at least 1 hour at room temperature (i.e. 22° ± 1°) and a pressure of 1 atmosphere. However, the oxidation process slows down as the film grows and is essentially self limiting, so that there is no upper limit to the useful time of exposure. Experiments in which an aluminium surface was exposed for two months resulted in a useful MIC polycrystalline layer, however practically speaking a period of 24 hours is usually employed. Increasing the temperature while the hydroxide film is growing will decrease the minimum time required.

If instead of an aluminium hydroxide film an aluminium oxide film is grown, the surface of the aluminium layer is exposed to a dry air atmosphere (0% relative humidity) for at least 6 hours at room temperature (i.e. 22° ± 1°) and a pressure of 1 atmosphere. As with hydroxide films, the process slows down as the film grows and is essentially self limiting so that there is no upper limit to the useful time of exposure. A period of 24 hours is usually employed. Again increasing the temperature while the oxide film is growing will decrease the minimum time required.

If forming a film which is a mixture of aluminium hydroxide and aluminium oxide, the surface of the aluminium layer is exposed to a semi-dry air atmosphere (0% < relative humidity < 100%) for at least 1 hour at room temperature (i.e. 22° ± 1°) and a pressure of 1 atmosphere. As with oxide and hydroxide films, the process slows down as the film grows and is again essentially self limiting with no upper limit to the useful time of exposure. A period of 24 hours is usually employed. Similarly, increasing the temperature while the oxide/hydroxide film is growing will decrease the minimum time required.

The term aluminium oxide, as used herein, should be understood to include any compound or complex containing aluminium and oxygen for example α-Al_2O_3 or γ-Al_2O_3. Similarly, the term aluminium hydroxide, as used herein, should be understood to include any compound or complex between aluminium, oxygen and hydrogen, for example: boehmite, pseudoboehmite, bayerite, or gibbsite.

For the Al-Si system, the Al and Al oxide and/or hydroxide etch is preferably performed with a phosphoric acid solution, using a 100% solution of 85% phosphoric acid, at about 130°C ± 3° for about 20 minutes ± 30 secs. Weaker solutions of phosphoric acid may also be used with a corresponding increase in etching time. Alternatively the etch may be performed with other acids such as hydrochloric acid.

Embodiments of the invention may make use of a lift-off process selected from the group comprising an acoustic treatment in de-ionized water or other solutions, a brush scrubbing process, or a hydrodynamic jet process.

Preferably the method will include a further processing step wherein, upon completion of the lift-off or doping step, a uniform surface treatment is performed to improve the surface finish of the sample prior to subsequent use of the semiconductor film for device fabrication or as a seed layer. The uniform surface treatment may be selected from the group comprising a KOH etch, a NaOH etch, a HF/HNO_3 etch, a H_3PO_4 etch, an argon plasma etch, or a combination of these.

The metal layer will be in the range of 30 – 500 nm thick and preferably 200 nm ± 10 % thick. The amorphous semiconductor layer used in the metal-induced crystallisation process is preferably greater in thickness than the metal layer and will preferably be in the range of 30 – 750 nm thick. When a 200 nm ± 10 % metal layer is used the amorphous semiconductor layer will be preferably 300 nm ± 10 % thick.

The metal-induced crystallisation step is preferably performed by annealing the sample at a temperature at or below 650°C and preferably at or below 500°C for 2 hours.

According to a second aspect, the present invention consists in a method of forming a film of polycrystalline semiconductor material on a supporting substrate of foreign material, the method comprising:

i. Forming a polycrystalline seed layer of a seed layer semiconductor material onto a target surface of the substrate on which the polycrystalline semiconductor film is to be formed;
ii. Cleaning the surface of the seed layer to remove any oxides or other contaminants;
iii. Forming, over the cleaned surface of the seed layer, an amorphous layer of the semiconductor material to become the polycrystalline film;
iv. Heating the substrate with the amorphous layer to crystallise the amorphous semiconductor material by solid phase epitaxy (SPE) to form the polycrystalline film ("SPE polycrystalline layer").

In preferred embodiments the polycrystalline film formed according to the first

aspect is used as the seed layer of the second aspect of the invention.

The amorphous layer may be undoped when formed but preferably dopant atoms may be added to the amorphous material as it is formed. Alternatively the semiconductor layer may be doped after it is formed as an amorphous layer or after it is crystallised.

In case of closely lattice matched crystalline semiconductor materials, the amorphous layer deposited on the clean surface of the crystalline seed layer and the seed layer itself can be different semiconductor materials ('hetero-epitaxial' solid phase epitaxy). One example of such a hetero-epitaxial process is solid phase epitaxy of germanium on a crystalline silicon seed layer. In this context, the crystalline semiconductor material can consist of an alloy between two or more semiconductor materials. The composition of the alloy can vary throughout the semiconductor film.

In preferred embodiments the amorphous semiconductor film is formed using a high-vacuum or ultra-high-vacuum electron-beam evaporation deposition process at a substrate temperature in the range of 20 – 650 °C and particularly preferred at a substrate temperature of 150 °C and a pressure in the range of $(0.2\text{-}1)\times10^{-7}$ Torr.

In the SPE crystallisation step, the substrate and amorphous layer are preferably heated to a temperature in the range of 200 – 650°C for a period of up to 7 days to crystallise the amorphous semiconductor material, and in a particularly preferred form of the invention the substrate and amorphous layer are heated to a temperature of 540 ± 5°C for a period of 17 ± 0.1 hours to crystallise the amorphous semiconductor material.

The amorphous semiconductor material layer may be doped n- and/or p-type during the semiconductor deposition process (i.e., *in-situ*). In the case of electron beam evaporation of the semiconductor material, this can be realised using resistively heated dopant effusion cells for n- and p-type dopants located in the vacuum electron-beam evaporation chamber.

The semiconductor material formed over the cleaned seed layer is preferably a material selected from the group comprising silicon, germanium, and an alloy of silicon and germanium.

Preferably also the step of cleaning the seed layer surface comprises the further steps of:

i. immersing the surface for 10 minutes in a fresh 1:1 mixture of hydrogen peroxide and sulfuric acid;
ii. rinsing the surface in de-ionized water;
iii. immersing the surface for 30 seconds in diluted (5%) hydrofluoric acid;

iv. immersing the surface in de-ionized water; and

v. drying the surface with gaseous nitrogen.

This process attaches hydrogen atoms to dangling bonds at the semiconductor surface, preventing oxidation of the surface for up to 60 minutes. Preferably the substrate is transferred to the semiconductor deposition chamber within 60 minutes of completion of the cleaning step to enable deposition onto an unoxidized surface and more preferably within 5 minutes.

The substrate is preferably a material selected from the group comprising quartz, glass (including float glass, borosilicate glass and other glass types), metal, graphite, ceramics, plastics and polymers.

In preferred embodiments the SPE polycrystalline layer is used to form a solar cell and the thickness of the layer is in the range of 0.5 to 3 μm. Preferably also electron beam evaporation is used as semiconductor deposition process and the amorphous material for this layer is deposited at a rate of up to 2 μm/min. Preferably also the deposition rate should be greater than 100 nm/min to minimise the impurity density (mainly oxygen, nitrogen and carbon) in the growing film caused by the vacuum chamber and its components. In the most preferred embodiment of the invention a deposition rate of about 250 ± 20 nm/min is used.

Brief Description of the Drawings

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings in which:

Fig. 1 illustrates a first step in fabrication of a thin-film polycrystalline layer where a silicon nitride (SiN) layer is deposited onto a clean, planar glass substrate;

Fig. 2 illustrates the sample of Fig. 1 after a thin (200 nm) aluminium layer is deposited (for example by evaporation) onto the SiN layer;

Fig. 3 illustrates the sample of Fig. 2 after the aluminium layer has been oxidized at room temperature, producing a thin aluminium oxide and/or hydroxide layer over the aluminium layer;

Fig. 4 illustrates the sample of Fig. 3 after a thin film (300 nm) of amorphous silicon (a-Si) has been deposited;

Fig. 5 illustrates the sample of Fig. 4 after the amorphous silicon has been crystallized by aluminium-induced crystallisation (AIC) at temperatures below 500°C for 2 hours in a nitrogen-purged atmospheric-pressure furnace, leaving a metal layer over the crystallised silicon and separated from it by a thin metal oxide and/or hydroxide layer, with crystalline silicon inclusions in the overlayer;

Fig. 6 illustrates the sample of Fig. 5 after the metal in the overlayer and the metal oxide and/or hydroxide film has been removed, leaving free-standing crystalline silicon islands on the AIC polycrystalline layer;

Fig. 7 illustrates the sample of Fig. 6 after the silicon islands have been removed by the lift-off step and a AIC polycrystalline silicon film with a wafer-like smooth surface has been obtained.

Fig. 8 shows a microscopical image (using a focussed ion beam (FIB) microscope) of the top surface of the sample of Fig. 7, demonstrating large crystal grain size.

Fig. 9 graphically illustrates a comparison between the measured reflectance of a high-quality commercial singlecrystalline silicon wafer and the AIC polycrystalline silicon film formed with an AIC process according to the present invention on planar glass;

Fig. 10 illustrates the sample of Fig. 7 after an amorphous n-type (800 nm thick) and ~5×10^{16} cm^{-3} phosphorus doped silicon layer and an amorphous n^+-type (100 nm and ~2×10^{19} cm^{-3} phosphorus doped) silicon layer have been deposited on the AIC polycrystalline silicon seed layer;

Fig. 11 illustrates the sample of Fig. 10 after a solid phase epitaxy (SPE) process has been performed to crystallise the amorphous silicon layers.

Fig. 12 schematically illustrates a vacuum evaporation chamber in which the amorphous layers seen in Fig. 10 are deposited by electron-beam evaporation and in-situ doped using resistively heated effusion cells for n- and p-type dopants;

Fig. 13 shows a FIB microscopical image of the surface of the sample of Fig. 11, demonstrating large crystal grain size; and

Fig. 14 graphically illustrates a comparison of the reflectances of a high-quality commercial singlecrystalline silicon wafer, the AIC polycrystalline silicon seed layer and the SPE polycrystalline silicon film shown in the microscopical image of Fig. 13.

Detailed Description of an Embodiment of the Invention

An embodiment of the invention will now be described which has demonstrated an ability to produce large-grained, island-free polycrystalline silicon with arbitrary doping on planar glass substrates. However, while the process is described for a silicon film on a glass substrate it will be appreciated that the process is also applicable to other semiconductors and foreign substrates.

The formation of a device-quality polycrystalline silicon layer on glass is a two-step process, the first of which is to form a high-quality seed layer and the second is to

form the device-grade layer over the seed layer. The formation of the seed layer involves the low-temperature (≤ 650°C) formation of a polycrystalline semiconductor film on a supporting substrate by means of metal-induced crystallisation (MIC) of amorphous films of the same semiconductor material and is schematically shown in Figures 1 and 6. The metal and semiconductor must be chosen such that they can form an eutectic system, and for the purpose of this example silicon and aluminium are used, however it will be recognised that other semiconductor/metal combinations can be selected from the groups of semiconductors and metals given above.

Referring to Fig. 1, the first step of the process is the deposition (for example by PECVD or reactive sputtering or reactive evaporation) of a silicon nitride (SiN) layer 22 onto a clean glass substrate 21. The SiN layer acts as a barrier layer for impurities from the glass and, if the thickness is suitably chosen, as an antireflection coating (AR coating). Next, as seen in Fig. 2, an approximately 200 nm thick aluminium layer 23 is deposited (for example by vacuum evaporation) onto the SiN layer 22. An aluminium hydroxide film 24 is then grown by exposing the aluminium layer 23 to an air atmosphere containing 100% relative humidity at room temperature (i.e. 22° ± 1°) for 24 hours at 1 atmosphere pressure, to produce the result as seen in Fig. 3.

Over the hydroxide film 24 is deposited about 300 nm of amorphous silicon 25 (a-Si) by sputtering (or evaporation or PECVD) as illustrated in Fig. 4. Layers 23, 24 & 25 are the pre-cursors for the aluminium-induced crystallization (AIC) process. The sample is then annealed at temperatures at or below 650° and preferably at or below 500°C for 2 hours in a nitrogen-purged atmospheric-pressure furnace to cause crystallisation of the amorphous silicon by the AIC process.

During the AIC process the aluminium and the silicon exchange the place and the a-Si is crystallised. Furthermore, on top of the 200 nm crystalline silicon 26 an overlayer 27 consisting of aluminium 29 and crystalline silicon inclusions 28 is formed, resulting in the arrangement seen in Figure 5. In addition, there is a thin (~30 nm) porous interfacial film 30 consisting of aluminium hydroxide and/or aluminium oxide between the polycrystalline silicon film 26 and the overlayer 27. The porous interfacial film 30 varies in thickness laterally and may contain a few pinpoint areas with direct contact between the polycrystalline silicon film 26 and the crystalline silicon inclusions 28. The crystalline silicon inclusions 28 are strongly connected to the underlying porous interfacial film 30 which is strongly connected to the underlying silicon film 26. Due to diffusion of Si through the interfacial film 30 during the AIC process, the interfacial film 30 may contain small amounts of Si contaminants.

The aluminium 29 and aluminium hydroxide and/or aluminium oxide film 30 of the overlayer 27 are etched off to achieve the state shown in Fig. 6. This etch preferably uses a phosphoric acid solution, comprising a 100% solution of 85% phosphoric acid at about 130°C for about 20 minutes. Weaker solutions of phosphoric acid may also be used, with a corresponding increase in etching time. This etch removes the aluminium hydroxide layer and/or aluminium oxide 30 without significantly etching the underlying polycrystalline silicon layer 26, and by means of lateral underetching, the etch also removes the aluminium hydroxide and/or aluminium oxide layer 30 below the silicon islands 28, thereby significantly decreasing the adhesion of the semiconductor islands 28 in Fig. 6.

The significantly decreased adhesion strength between the silicon islands 28 and the polycrystalline layer 26 makes possible a simple lift-off process to achieve removal of the silicon islands. A cleaning sequence is used to effect lift-off of the silicon islands 28, an example being ultrasonic treatment in deionized water in combination with a brush scrubbing process of the sample of Figure 6, to thereby produce a polycrystalline silicon film with uniform thickness on the substrate. An additional, optional, processing step is a uniform surface treatment that improves the surface finish of the sample prior to subsequent device fabrication or use as a seed layer. Figure 7 shows a schematic representation of a sample prepared to this stage in accordance with an embodiment of the present invention.

The sample seen in Fig. 7, which is a polycrystalline silicon film formed with the above AIC process on planar glass, shows a wafer-like smooth surface, and as seen in the FIB (focused ion beam) picture of Fig. 8 the grains of the polycrystalline silicon film are up to 20 μm wide, with an average width of about 10 μm. It is anticipated that grain sizes of up to 100 μm or more can be expected to be produced by this process. Experimentation has shown that a Si island free surface such as this is a key requirement for high material quality in the subsequent solid phase epitaxy step. The AIC polycrystalline silicon film shown in Fig. 7 is of exceptional material quality and highly p-type due to the Al content of about 2×10^{19} cm^{-3}. If a doping polarity change is desired, the sample can be heated to 900°C, for up to 5 minutes, in the vicinity of an *n*-type spin-on doping source. An *n*-type AIC polycrystalline silicon film can then be formed with a low resistivity in the order of 0.002 Ωcm. To prevent sticking of the glass, a graphite substrate holder is preferably used during the high-temperature anneal.

The UV reflectance of a silicon sample is a direct measure of its material quality. The reflectance of the sample seen in Fig. 7 was measured and compared with that of a high-quality commercial singlecrystalline silicon wafer. The results of that

comparison can be seen in the graph of Fig. 9. The difference is less than 2 % and clearly demonstrates the good material quality of the AIC film.

To fabricate a solar cell from the ~200 nm crystalline Si layer (a so-called "seed layer") produced by the process described above, the silicon must be thickened to a total of 0.5-3 μm to absorb most of the incident sunlight. In the subsequent solid phase epitaxy step the crystalline information of the seed layer is exploited and transferred into the subsequently formed crystalline layers.

To create a contamination and oxide free interface on the crystalline silicon seed layer 26, which is a crucial requirement for epitaxy, the seed layer is first immersed for 10 minutes in a fresh 1:1 mixture of hydrogen peroxide and sulfuric acid, followed by a rinse in de-ionized water, then immersed for 30 seconds in diluted (5%) hydrofluoric acid, then immersed in de-ionized water and then dried with gaseous nitrogen (using a "nitrogen gun"). The samples are then immediately transferred into the amorphous silicon deposition apparatus. The chemical procedure described above creates a hydrogen-terminated silicon surface (i.e., hydrogen atoms are bonded to the silicon surface atoms), which suppresses the re-growth of a silicon oxide film on the surface for quite some time (in order of 30 minutes at room temperature).

Using a high-vacuum electron-beam evaporation process, an amorphous n- or p-type (~5×10^{16} cm^{-3} phosphorus or gallium) silicon layer 31 and an amorphous n^+-type (~2×10^{19} cm^{-3} phosphorus) silicon layer 32 are deposited at approximately 150°C in one run (i.e., without interrupting the silicon deposition) to produce the structure seen in Fig. 10. The combined thickness of layers 31 and 32 is approximately 1 μm and is deposited at a rate of about 250 nm/min. Both the high rate and the high vacuum ensure semiconductor-grade material, which is essential for solar cells. The high rate allows the whole structure to be formed within less than 10 minutes. Other methods like PECVD need much longer for the same thickness.

Referring to Fig. 12, the high-vacuum evaporation process is performed in an electron-beam evaporator for silicon evaporation 41 comprising a high-vacuum chamber 42 which is continuously evacuated using a high-vacuum pump 43. The high-vacuum pump 43 operates through a valve 44 which, to avoid damage to the high-vacuum pump 43, is only open if the chamber pressure is below the maximum operating pressure of the pump. The chamber is pumped down to this maximum pressure by a second, low-vacuum pump (not shown). In operation a base pressure of 5×10^{-7} Torr or lower is required to ensure low contamination levels in the deposited amorphous silicon. The sample 45 is transferred into the chamber via a loadlock 58 and then heated to the desired temperature by halogen lamps 46 enclosed in a

molybdenum housing 47. A valve 59 between the loadlock 58 and the chamber 42 is used to separate the chamber 42 from the loadlock 58 while the loadlock is pumped down to a pressure of below the maximum operation pressure of the high-vacuum pump 43. The valve 59 is preferably opened at pressures in the loadlock 58 which are low enough to minimise the contamination of the chamber 42. As shown in Fig. 12 the sample 45 is heated from the back side (i.e. through the glass substrate) and the silicon side is oriented to face the melting pot 48 which holds solid silicon for thermal evaporation and subsequent deposition on the surface of the sample 45. The silicon within the melting pot is melted by an electron beam 56 created by an electron gun 55 and directed onto the silicon source material 57 using magnetic fields (not shown). There are additionally two resistively heated effusion cells 49, 51 for in-situ gallium and phosphorus doping during deposition. A shutter 52 is positioned between the sample and the e-beam evaporator to shield the sample until the silicon deposition process is ready to commence.

The structure of Fig. 10 is the pre-cursor for the following crystallisation step known as (homo-epitaxial) solid phase epitaxy (SPE). If a hetero-epitaxial SPE process is desired, the silicon within the melting pot is replaced by germanium for example and subsequently melted by the electron beam 56 created by the electron gun 55 as described above. If hetero-epitaxial SPE of a silicon-germanium alloy is desired, two separate melting pots can be used, one for silicon and one for germanium materials, and by the way of co-evaporation the amorphous silicon-germanium alloy to be crystallised by hetero-epitaxial SPE is deposited on the polycrystalline silicon seed layer.

The SPE process is performed by a lamp-heated vacuum annealing process at about 540°C, whereby the halogen lamps 46 illuminate the silicon through the glass substrate 21. This process can be performed with a significantly reduced vacuum to that of the deposition step and a vacuum of 5×10^{-6} Torr is adequate. Alternatively, the SPE process may be performed in a nitrogen-purged atmospheric-pressure furnace. The doped amorphous silicon layers 31 and 32 of Fig. 10 fully crystallize within 17 hours, starting from the underlying AIC seed layer, to produce the structure of Fig. 11, in which the obtained doped crystalline silicon layers 33 and 34 have a similar crystalline structure and material quality as that of the seed layer 26. For certain device applications (for example solar cells) it is necessary to increase the fraction of electrically active dopant atoms by subjecting the sample to a short (< 5 minutes) high-temperature anneal in the range 700 - 1000 °C. To prevent sticking of the glass, a graphite substrate holder is preferably used during the high-temperature anneal. The thermal budget of such a rapid thermal process is small enough to make it compatible

with commercially available glass substrates. The FIB picture seen in Fig. 13 shows similarly large grains as those seen in the thin crystalline seed layer (see Fig. 8). Also no surface roughness is visible in the FIB image.

Referring to Fig. 14, the UV reflectance measured on the sample of Figure 13 (dashed curve in Fig. 14) shows very similar characteristics to that of the AIC seed layer 26 (dotted curve in Fig. 14). The small differences that are apparent are believed to be due to an oxide present on the surface of the finished silicon film, which was not removed prior to the reflectance measurement.

Sample	Peak (cm^{-1})	FWHM (cm^{-1})	Intensity
Silicon reference	518.9 ± 0.2	6.3 ± 0.2	10700 ± 500
AIC seed layer	522.2 ± 0.6	6.8 ± 0.2	1800 ± 100
Finished film	519.2 ± 0.3	6.7 ± 0.4	6200 ± 1600

Table 1

Since both FIB and UV reflectance exclusively probe the near-surface region of a sample, Raman measurements were performed on a silicon wafer reference, the AIC seed layer, and the finished device. Raman measurements probe the material quality of the bulk of the films (penetration depth of used Raman laser light ca. 1-2 μm). High intensity but mostly narrow peaks were observed, which are clear signs of good material quality. The full width at half maximum (FWHM) of the fabricated sample differs only marginally from the silicon wafer reference and is only slightly lower in intensity, which can be attributed to the lower thickness of the fabricated film. Results of the Raman measurements can be seen in Table 1.

The low thermal budget (which is compatible with commercial glass), the high deposition rate for the deposition of the main material (layers 31/33 and 32/34) and the simplicity of the process, which does not include the use of toxic gasses, make it a very attractive technique for industrial applications.

It will be appreciated by persons skilled in the art that numerous variations and/or modifications may be made to the invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive.

Claims:

1. A method of forming a polycrystalline semiconductor film on a supporting substrate of foreign material, the method comprising:

i. Depositing a metal film onto a target surface of the substrate on which the polycrystalline semiconductor film is to be formed;

ii. Forming a film of metal oxide and/or metal hydroxide on a surface of the metal;

iii. Forming a layer of an amorphous semiconductor material over a surface of the metal oxide and/or metal hydroxide film;

iv. Heating the substrate, the metal, the metal oxide and/or metal hydroxide film and the amorphous semiconductor material to a temperature at which the semiconductor layer is absorbed into the metal layer and deposited onto the target surface by metal-induced crystallisation (MIC) as a polycrystalline layer, whereby the metal is left as an overlayer covering the deposited polycrystalline layer, with semiconductor inclusions in the metal layer, and the polycrystalline semiconductor film and the overlayer separated by a porous interfacial metal oxide and/or metal hydroxide film, with which the semiconductor inclusions are in contact;

v. Removing the metal in the overlayer and the interfacial metal oxide and/or metal hydroxide film with an etch which underetches the semiconductor inclusions to form freestanding islands weakly connected to the polycrystalline layer, without significantly thinning the underlying polycrystalline semiconductor layer;

vi. Removing the freestanding semiconductor "islands" from the surface of the polycrystalline semiconductor layer by a lift-off process.

2. The method of claim 1 wherein the substrate provides a planar base on which the semiconductor material is supported.

3. The method of claim 1 or 2 wherein a surface on which the semiconductor material is supported is textured to assist light trapping in the semiconductor material.

4. The method of claim 1, 2 or 3 wherein the substrate comprises a sheet of substrate material over which a preliminary layer is deposited and the target surface is a surface of the preliminary layer.

5. The method of claim 4 wherein which the preliminary layer is a silicon nitride or aluminium oxide or silicon oxide film.

6. The method as claimed in any one of claims 1 to 5 wherein, as a result of the MIC step, metal atoms are left in the polycrystalline layer which act as dopants and after the lift-off process, the polycrystalline semiconductor layer is doped with a dopant which overcompensates the doping caused by the metal atoms left in the polycrystalline layer after the MIC step, thereby causing the polycrystalline semiconductor layer to have an overall doping polarity which is opposite to that which would occur due to the metal atoms alone.

7. The method of claim 6 wherein the dopant overcompensation is achieved by depositing a spin-on dopant film onto the polycrystalline semiconductor film, heating of the sample, and removal of the spin-on dopant film.

8. The method of claim 6 wherein the dopant overcompensation is achieved by heating of the polycrystalline semiconductor layer in a gas atmosphere containing dopant atoms.

9. The method as claimed in any one of claims 1 to 5 wherein, as a result of the MIC step, metal atoms are left in the polycrystalline layer which act as dopants and the amorphous semiconductor material is doped during its formation with atoms that produce an opposite-polarity doping when compared to the polarity of doping caused by the metal atoms left in the polycrystalline layer after the MIC step, the opposite polarity doping being sufficient to overcompensate for the presence of the metal atoms whereby after the MIC step the net doping is opposite in polarity to that which would be produced by the metal atoms alone.

10 The method as claimed in any one of claims 1 to 9, wherein the substrate is a material selected from the group comprising sapphire, quartz, glass (including float glass, borosilicate glass and other glass types), metal, graphite, ceramics, plastics and polymers.

11. The method as claimed in any one of claims 1 to 10, wherein the polycrystalline semiconductor film is of a semiconductor material selected from the group comprising silicon, germanium, and an alloy of silicon and germanium.

12. The method as claimed in any one of claims 1 to 11 wherein the metal is selected such that the metal forms a eutectic solution with the selected semiconductor.

13. The method of claim 12 wherein the metal is selected from the group of metals comprising Be, Al, Zn, Ga, Ag, Cd, In, Sn, Sb and Au.

14. The method of claim 13 wherein the semiconductor is silicon and the metal is aluminium.

15. The method of claim 14 wherein an aluminium hydroxide film is formed by exposing the aluminium layer to an air atmosphere containing 100% relative humidity at room temperature (22° ± 1°) for more than 1 hour at 1 atmosphere pressure.

16. The method of claim 14 wherein an aluminium hydroxide film is formed by exposing the aluminium layer to an air atmosphere containing 100% relative humidity at room temperature (22° ± 1°) for at least 24 hours at 1 atmosphere pressure.

17. The method of claim 14 wherein an aluminium oxide film is formed by exposing the aluminium layer to a dry air atmosphere (i.e. containing 0% relative humidity) at room temperature (22° ± 1°) for more than 6 hours at 1 atmosphere pressure.

18. The method of claim 14 wherein an aluminium hydroxide film is formed by exposing the aluminium layer to a dry air atmosphere (i.e. containing 0% relative humidity) at room temperature (22° ± 1°) for at least 24 hours at 1 atmosphere pressure.

19. The method of claim 14 wherein a film comprising a mixture of aluminium hydroxide and aluminium oxide is formed by exposing the aluminium layer to a semi-dry air atmosphere containing a relative humidity of more than 0% and less than 100% at room temperature (22° ± 1°) for more than 1 hour at 1 atmosphere pressure.

20. The method of claim 14 wherein a film comprising a mixture of aluminium hydroxide and aluminium oxide is formed by exposing the aluminium layer to a semi-dry air atmosphere containing a relative humidity of more than 0% and less than 100% at room temperature (22° ± 1°) for at least 24 hours at 1 atmosphere pressure.

21. The method as claimed in any one of claims 1 to 20 wherein the metal and metal oxide and/or metal hydroxide etch is performed with a phosphoric acid solution.

22. The method of claim 21 wherein the phosphoric acid solution is a 100% solution of 85% phosphoric acid, and the etch is performed at 130°C ± 3°C for 20 minutes ± 30 seconds.

23. The method as claimed in any one of claims 1 to 22 wherein the lift-off process is selected from the group comprising an acoustic treatment in a solution bath, a brush scrubbing process, or a hydrodynamic jet process.

24. The method as claimed in any one of claims 1 to 23 wherein the lift-off process is an brush scrubbing process.

25. The method as claimed in any one of claims 1 to 24 wherein the method further includes the step of, upon completion of the lift-off process, performing a uniform surface treatment to improve the surface finish of the sample prior to subsequent use of the semiconductor film.

26. The method of claim 25 wherein the further step is an etch step comprising one or more etches selected from the group comprising a KOH etch, an NaOH etch, a HF/HNO_3 etch, a H_3PO_4 etch and an argon plasma etch.

27. The method as claimed in any one of claims 1 to 26 wherein the metal layer has a thickness in the range of 30 – 500 nm.

28. The method as claimed in any one of claims 1 to 27 wherein the amorphous semiconductor layer used in the metal-induced crystallisation process has a thickness in the range of 30 – 750 nm.

29. The method of claim 28 wherein the metal layer has a thickness of 200 nm ± 10 % and the amorphous semiconductor layer has a thickness of 300 nm ± 10 %.

30. The method as claimed in any one of claims 1 to 29 wherein the metal-induced crystallisation is performed by annealing the sample at a temperature of 650 °C or less.

31. The method of claim 30 wherein the metal-induced crystallisation is performed by annealing the sample at a temperature of 500 °C or less for 2 hours.

32. The method as claimed in any one of claims 1 to 31, wherein the polycrystalline layer formed by metal-induced crystallisation on a foreign substrate is used as a seed layer for the formation of a further polycrystalline layer, the method further comprising:

Cleaning the surface of the seed layer to remove any oxides or other contaminants;

Forming a second amorphous layer of a semiconductor material over the cleaned surface of the seed layer;

Heating the substrate, the seed layer and the second amorphous layer to crystallise the semiconductor material by solid phase epitaxy (SPE).

33. The method as claimed in claim 32 wherein the semiconductor material of the seed layer and the second amorphous layer are of the same semiconductor material with the same or different doping.

34. The method as claimed in claim 32 wherein the semiconductor material of the seed layer and the second amorphous layer are different semiconductor materials.

35. The method as claimed in claim 32 or 34 wherein the semiconductor material of the second amorphous layer is germanium or an alloy of silicon and germanium.

36. The method of claim 35 wherein the substrate, the seed layer and the second amorphous layer are heated to a temperature in the range of 200 – 650 °C to crystallise the semiconductor material by SPE.

37. The method as claimed in claim 32 or 33 wherein the second amorphous layer is silicon.

38. The method of claim 37 wherein the substrate, the seed layer and the second amorphous layer are heated to a temperature in the range of 520 – 560 °C for a period in the range of 15 to 20 hours to crystallise the semiconductor material.

39. The method of claim 38 wherein the substrate, the seed layer and the second amorphous layer are heated to a temperature of 540 ± 5°C for a period of 17 ± 0.1 hours to crystallise the semiconductor material.

40. The method as claimed in any one of claims 32 to 39 wherein the second amorphous layer is simultaneously doped as it is formed.

41. The method of claim 37, 38 or 39 wherein the second amorphous layer is simultaneously and progressively doped with gallium and then phosphorus as it is formed.

42. The method of claim 37, 38 or 39 wherein the second amorphous layer is simultaneously and progressively doped with boron and then phosphorus as it is formed.

43. The method as claimed in any one of claims 32 to 42 wherein the second amorphous semiconductor layer is formed by plasma enhanced chemical vapour deposition, sputtering, chemical vapour deposition, resistively heated evaporation or electron beam evaporation.

44. The method as claimed in any one of claims 32 to 42 wherein the second amorphous semiconductor layer is formed in a vacuum electron beam evaporation process at a temperature of 20 - 400 °C.

45. The method of claim 44 wherein the second amorphous semiconductor layer is formed in a vacuum electron beam evaporation process at a temperature of 150 °C ± 20 °C and at a pressure of less than 5×10^{-7} Torr.

46. The method of claim 45 wherein the semiconductor deposition process to deposit the second amorphous semiconductor layer is performed at a pressure of less than 1×10^{-7} Torr.

47. The method of claims 44, 45 or 46 wherein the second amorphous semiconductor layer is formed in a electron beam evaporation process with a deposition rate of up to 2 μm/min.

48. The method as claimed in any one of claims 44 to 47 wherein the second amorphous semiconductor layer is deposited at a rate of 100 nm/min or more.

49. The method of claim 48 wherein the second amorphous semiconductor layer is formed in an electron beam evaporation process with a deposition rate of 250 ± 20 nm/min.

50. The method as claimed in any one of claims 32 to 49 wherein the amorphous semiconductor material of the second amorphous semiconductor layer is doped to a predetermined doping profile during an electron beam evaporation deposition process using resistively heated p-type and n-type dopant effusion cells in the vacuum electron-beam evaporation chamber while the deposition process takes place.

51. The method as claimed in any one of claims 32 to 50 wherein the substrate, the seed layer and the second amorphous semiconductor layer are heated in a vacuum furnace.

52. The method as claimed in any one of claims 32 to 50 wherein the substrate, the seed layer and the second amorphous semiconductor layer are heated in an atmospheric furnace.

53. The method as claimed in any one of claims 32 to 52 wherein the substrate, the seed layer and the second amorphous semiconductor layer are heated by radiative heating.

54. The method as claimed in any one of claims 37 to 39, 41, or 42 wherein the step of cleaning the seed layer surface comprises a process which creates a hydrogen-terminated silicon surface and the substrate is transferred to the semiconductor deposition chamber within 60 minutes of completion of the cleaning step.

55. The method of claim 54 wherein the step of cleaning the seed layer surface comprises the further steps of:

i. immersing the surface for 10 minutes in a fresh 1:1 mixture of hydrogen peroxide and sulfuric acid ;
ii. rinsing the surface in de-ionized water;
iii. immersing the surface for 30 seconds in diluted (5%) hydrofluoric acid;
iv. immersing the surface in de-ionized water; and
v. drying the surface with gaseous nitrogen.

56. The method as claimed in any one of claims 37 to 39, 41, 42, 54 or 55 wherein after the step of crystallisation by solid phase epitaxy, a further high-temperature anneal is performed at a temperature in the range 700 - 1000 °C for a period of less than five minutes to increase the fraction of electrically active dopant atoms in the crystalline semiconductor material.

57. A method of forming a film of polycrystalline semiconductor material on a supporting substrate of foreign material, the method comprising:

i. Forming a polycrystalline seed layer of a seed layer semiconductor material onto a target surface of the substrate on which the polycrystalline semiconductor film is to be formed.

ii. Cleaning the surface of the seed layer to remove any oxides or other contaminants;

iii. Forming over the cleaned surface of the seed layer an amorphous layer of the semiconductor material to become the polycrystalline film;

iv. Heating the substrate, the seed layer and the amorphous layer to crystallise the amorphous semiconductor material by solid phase epitaxy (SPE).

58. The method of claim 57 wherein the substrate provides a planar base on which the semiconductor material is supported.

59. The method of claim 57 or 58 wherein a surface on which the semiconductor material is supported is textured to assist light trapping in the semiconductor material.

60. The method of claims 57, 58 or 59 wherein the step of forming the amorphous layer of semiconductor material over the cleaned surface of the seed layer comprises forming an amorphous semiconductor layer by evaporation.

61. The method of claim 60 wherein the step of forming the amorphous layer of semiconductor material over the cleaned surface of the seed layer comprises placing the substrate in a high-vacuum electron-beam evaporation chamber with a source of the semiconductor material and forming an amorphous layer of the semiconductor material over the cleaned surface of the seed layer using a high-vacuum, electron-beam evaporation deposition process;

62. The method of claims 57, 58 or 59 wherein the step of forming the amorphous layer of semiconductor material over the cleaned surface of the seed layer comprises forming an amorphous semiconductor layer by plasma enhanced chemical vapour deposition.

63. The method of claims 57, 58 or 59 wherein the step of forming the amorphous layer of semiconductor material over the cleaned surface of the seed layer comprises forming an amorphous semiconductor layer by sputtering.

64. The method of claims 57, 58 or 59 wherein the step of forming the amorphous layer of semiconductor material over the cleaned surface of the seed layer comprises forming an amorphous semiconductor layer by chemical vapour deposition,

65. The method as claimed in any one of claims 57 to 64 wherein the substrate comprises a sheet of substrate material over which a preliminary layer is deposited and the target surface is a surface of the preliminary layer.

66. The method of claim 65 wherein which the preliminary layer is a silicon nitride or aluminium oxide or silicon oxide film.

67. The method as claimed in any one of claims 57 to 66, wherein the second amorphous layer is silicon.

68. The method as claimed in claim 67 wherein the substrate, the seed layer and the amorphous semiconductor layer are heated to a temperature in the range of 520 – 560 °C for a period in the range of 15 to 20 hours to crystallise the amorphous semiconductor material.

69. The method of claim 68 wherein the sample is heated to a temperature of 540 ± 5 °C for a period of 17 ± 0.1 hours to crystallise the amorphous semiconductor material.

70. The method as claimed in any one of claims 57 to 65 wherein the semiconductor material of the second amorphous layer is germanium or an alloy of silicon and germanium.

71. The method of claim 70 wherein the substrate, the seed layer and the second amorphous layer are heated to a temperature in the range of 200 – 650 °C to crystallise the semiconductor materia by SPE.

72. The method as claimed in any one of claims 67 to 69 wherein the amorphous silicon layer is formed at a temperature of 20 - 400 °C.

73. The method as claimed in any one of claims 57 to 72 wherein the semiconductor material of the seed layer and the SPE polycrystalline layer are the same semiconductor material with the same or different doping.

74. The method as claimed in any one of claims 57 to 72 wherein the semiconductor material of the seed layer and the SPE polycrystalline layer are different semiconductor materials.

75. The method as claimed in any one of claims 57 to 74 wherein the amorphous layer is simultaneously doped as it is formed.

76. The method of claim 67, 68, 69 or 72 wherein the amorphous layer is simultaneously and progressively doped with gallium and then phosphorus as it is formed.

77. The method of claim 67, 68, 69 or 72 wherein the amorphous layer is simultaneously and progressively doped with boron and then phosphorus as it is formed.

78. The method of claim 72, 76 or 77 wherein the amorphous layer is formed at a temperature of 150 °C+/- 20 °C and at a pressure of less than 5×10^{-7} Torr.

79. The method of claim 78 wherein the semiconductor deposition process to deposit the amorphous layer is performed at a pressure of less than 1×10^{-7} Torr.

80. The method as claimed in any one of claims 57 to 79 wherein the amorphous layer is formed in an electron beam evaporation process with a deposition rate of up to 2 μm/min.

81. The method of claim 80 wherein the amorphous layer is deposited at a rate of 100 nm/min or more.

82. The method of claim 80 or 81 wherein the amorphous layer is formed with a deposition rate of 250 ± 20 nm/min.

83. The method as claimed in any one of claims 57 to 85 wherein the semiconductor material of the amorphous layer is doped to a predetermined doping profile during the deposition process using resistively heated p-type and n-type dopant effusion cells in the vacuum electron-beam evaporation chamber while the deposition process takes place.

84. The method as claimed in any one of claims 57 to 83 wherein the substrate, the seed layer and the amorphous semiconductor layer are heated in a vacuum.

85. The method as claimed in any one of claims 57 to 83 wherein the substrate, the seed layer and the amorphous semiconductor layer are heated in an atmospheric furnace.

86. The method as claimed in any one of claims 57 to 85 wherein the substrate, the seed layer and the amorphous semiconductor layer are heated by radiative heating.

87. The method as claimed in any one of claims 67, 68, 69, 72, 76, 77, 78, or 79 wherein the semiconductor material is silicon and the cleaning step comprises a process which creates a hydrogen-terminated silicon surface and the substrate is transferred to the semiconductor deposition chamber within 60 minutes of completion of the cleaning step.

88. The method of claim 87 wherein the step of cleaning the seed layer surface comprises the further steps of: -

vi. immersing the surface for 10 minutes in a fresh 1:1 mixture of hydrogen peroxide and sulfuric acid;

vii. rinsing the surface in de-ionized water;

viii. immersing the surface for 30 seconds in diluted (5%) hydrofluoric acid;

ix. immersing the surface in de-ionized water; and

x. drying the surface with gaseous nitrogen.

89. The method as claimed in any one of claims 57 to 88 wherein the substrate is a material selected from the group comprising quartz, glass (including float glass, borosilicate glass and other glass types), metal, graphite, ceramics, plastics and polymers.

90. The method as claimed in any one of claims 67, 68, 69, 72, 76, 77, 78, 79 or 88 wherein after the step of crystallisation by solid phase epitaxy, a further high-temperature anneal is performed at a temperature in the range 700 - 1000 °C for a period of less than five minutes to increase the fraction of electrically active dopant atoms in the crystalline semiconductor material.

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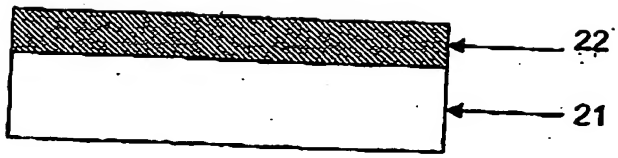

Fig. 1

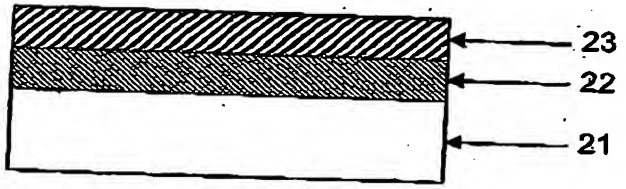

Fig. 2

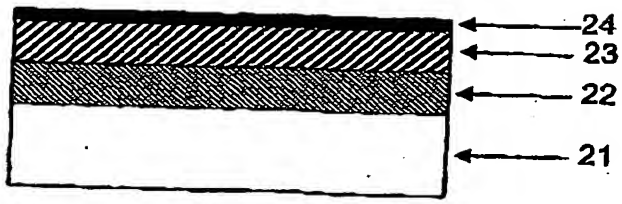

Fig. 3

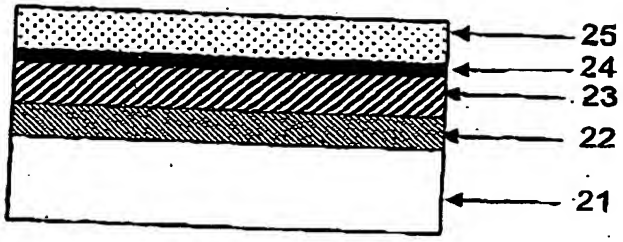

Fig. 4

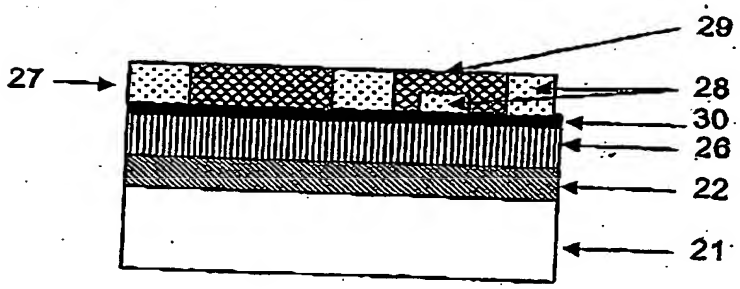

Fig. 5

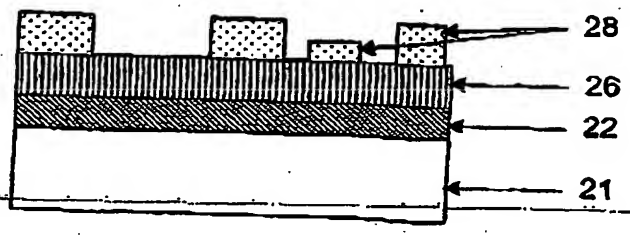

Fig. 6

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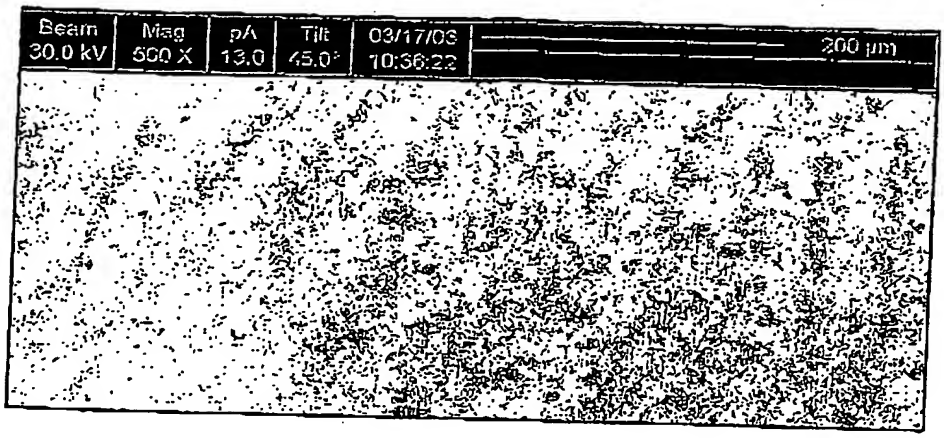

Fig. 8

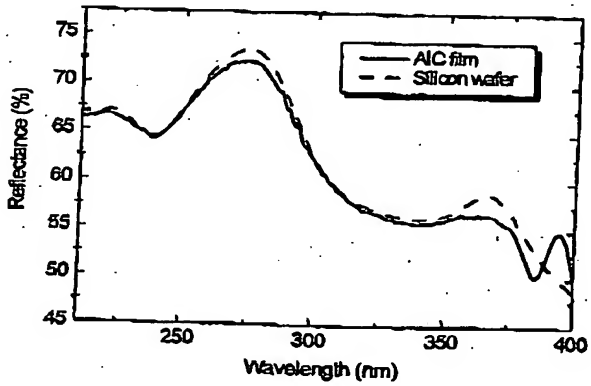

Fig. 9

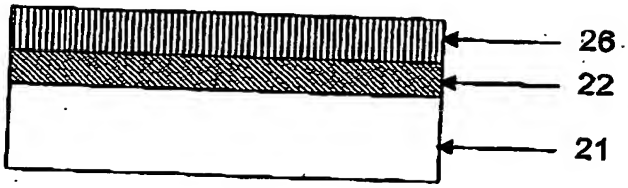

Fig. 7

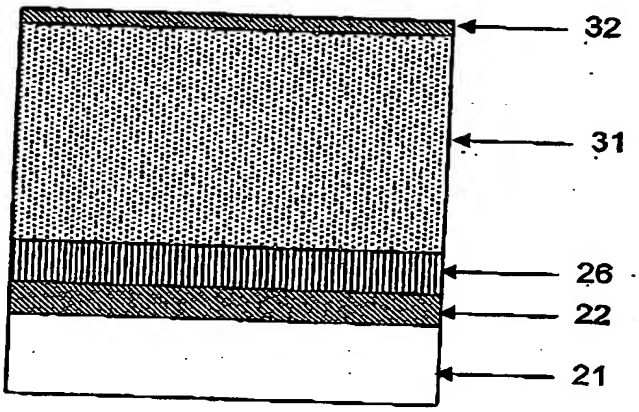

Fig. 10

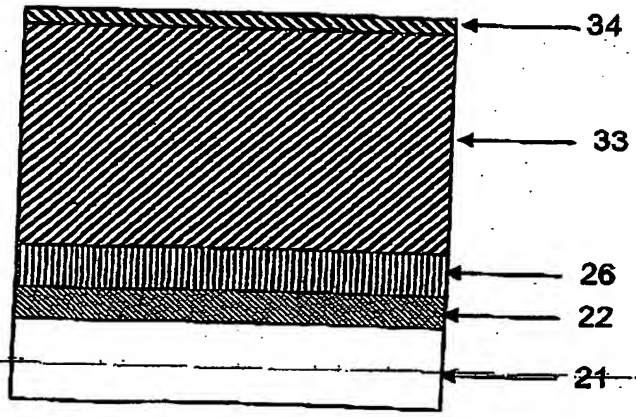

Fig. 11

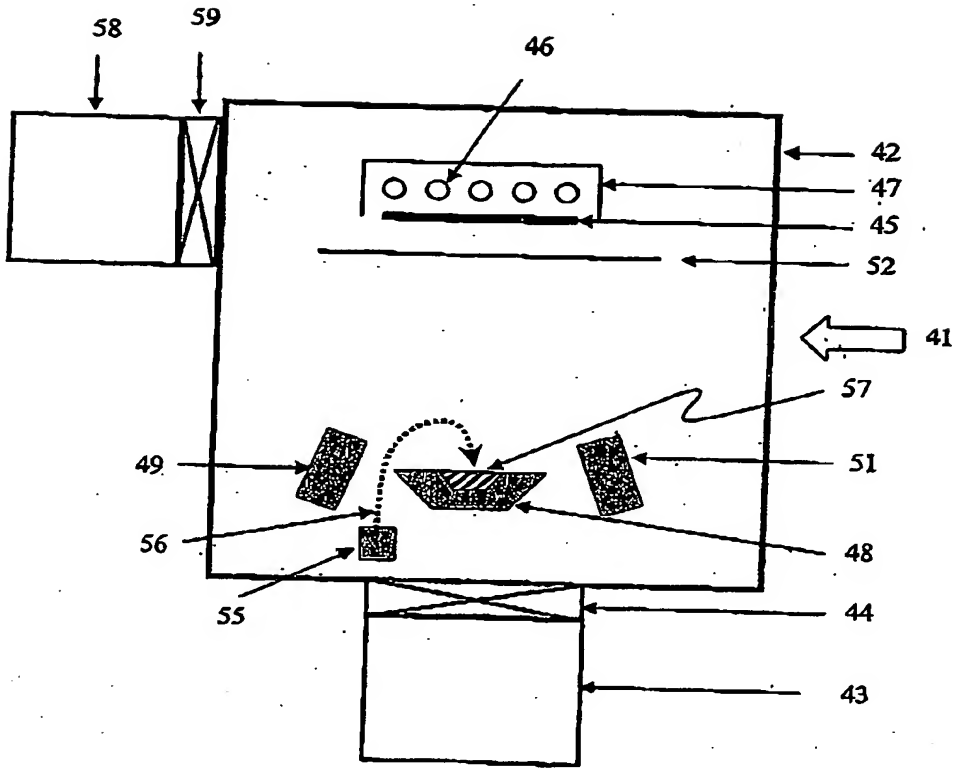

Fig. 12

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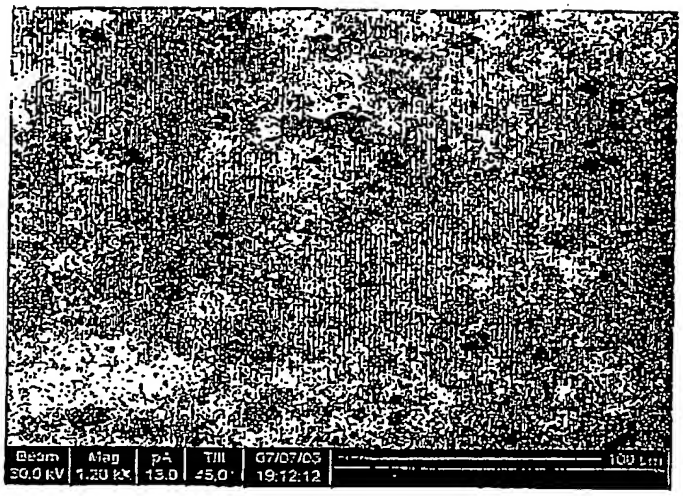

Fig. 13

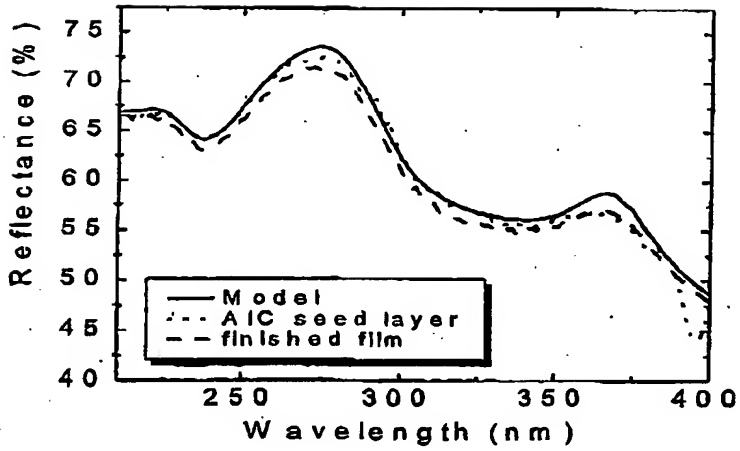

Fig. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU03/01313

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. [7]: C30B 28/02, 29/06, H01L 31/18, 21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI, JAPIO: (polysilicon, poly silicon, polycrystalline semiconductor, polycrystalline silicon etc), (amorphous semiconductor etc), (heat+, thermal+, anneal+), (metal induced crystalli+), (metal or aluminium etc (s) layer+ or film?), (heteroepitax+), (+etch+), (seed+ or nucleat+ (s) layer+ or film?), (thermal budget), (remov+ or clean+ (s) surface), (form+, deposit+, grow+), (inclusion? or island?), (solid phase epitaxy, spe), overlayer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6383851 B2 (PING) 7 May 2002 See the abstract, col 3 line 20-40	57-90
X	US 6251715 B1 (JUNG et al) 26 June 2001 See the abstract	57-90
X	US 5344796 A (SHIN et al) 6 September 1994 See the abstract	57-90

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 December 2003	23 DEC 2003
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized officer I.A.BARRETT Telephone No : (02) 6283 2189

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU03/01313

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6451637 B1 (JANG et al) 17 September 2002 See the abstract	
A	US 6248675 B1 (XIANG et al) 19 June 2001 See the abstract	
A	US 5275851 A (FONASH et al) 4 January 1994 See the abstract, col 3 line 16-41	
A	EP 1271620 A1 (KIM) 2 January 2003 See the abstract	
A	Journal of Crystal Growth, Volume 242, Issues 3-4, issued July 2002, (Elsevier), WIDENBORG et al, "Surface Morphology of poly-Si films made by aluminium-induced crystallisation on glass substrates", pages 270-282	
A	Solar Energy Materials and Solar Cells, Volume 69, Issue 2, issued September 2001, (Elsevier), NIIRA et al, "Thin film poly-Si formation for solar cells by Flux method and Cat-CVD method", pages 107-114	
A	Applied Physics Letters, Volume 73, Number 22, issued 30 November 1998, (American Institute of Physics), NAST et al, "Aluminum-induced crystallisation of amorphous silicon on glass substrates above and below the eutectic temperature", pages 3214-3216	
A	Journal of Applied Physics, Volume 88, Number 2, issued 15 July 2000, (American Institute of Physics), NAST et al, "Influence of interface and Al structure on layer exchange during aluminum-induced crystallization of amorphous silicon", pages 716-724	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU03/01313

Box I Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos :
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos :
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos :
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box II Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

There are two inventions covered by claims 1-56 and 57-90. Both methods relate to formation of polycrystalline semiconductor layers.

Continued on extra sheet.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims
2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU03/01313

Supplemental Box
(To be used when the space in any of Boxes I to VIII is not sufficient)

Continuation of Box No:

The method of claims 1-56 is characterised by special technical features :-

(a) depositing a metal film onto a target surface

(b) forming a metal oxide or hydroxide film on the metal layer

(c) forming a layer of amorphous semiconductor material over the metal oxide or hydroxide

(d) heating to form a polycrystalline semiconductor layer by metal induced crystallisation

(e) removing metal and metal oxide or hydroxide from an overlayer over the polycrystalline semiconductor layer

(f) removing freestanding semiconductor "islands" from the surface of the polycrystalline semiconductor layer.

The method of claims 57-90 is characterised by special technical features :-

(g) forming a polycrystalline semiconductor seed layer on a target surface

(h) cleaning the surface of the seed layer

(i) forming an amorphous semiconductor layer over the seed layer

(j) heating to crystallise the amorphous semiconductor layer by solid phase epitaxy.

Both methods relate to formation of polycrytalline semiconductor layers from amorphous semiconductor layers which is well known in the prior art and acknowledged in the description. While both methods result in a polycrystalline semiconductor layer, there do not appear to be any special technical features linking the two methods.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/AU03/01313

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	6383851	US	6204156	US	2001009799	US	2002115243
US	6251715	US	5858820				
US	5344796	JP	6204137				
US	6451637	KR	2000008068	KR	2000026624	KR	2000052007
		US	2002098297				
US	6248675						
US	5275851						
EP	1271620	JP	2003007638	US	2003010775		

END OF ANNEX